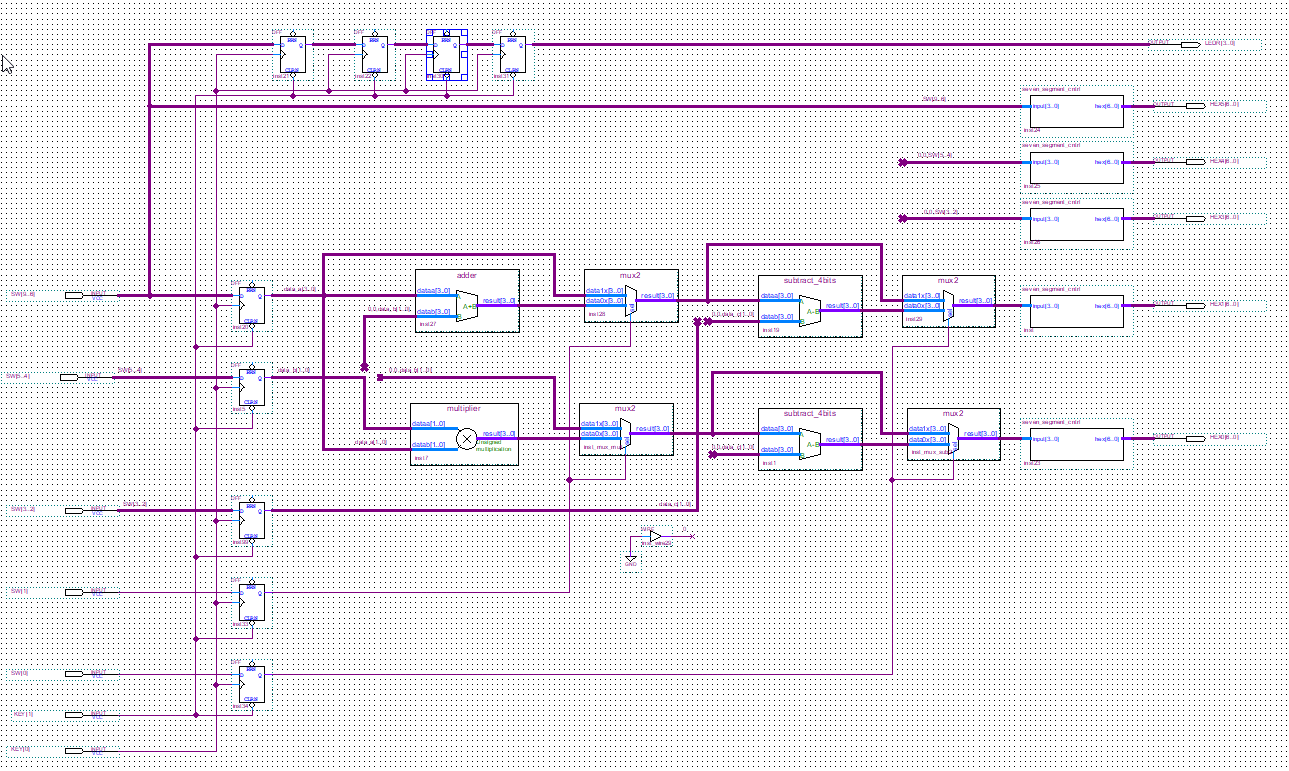
# Introduction:

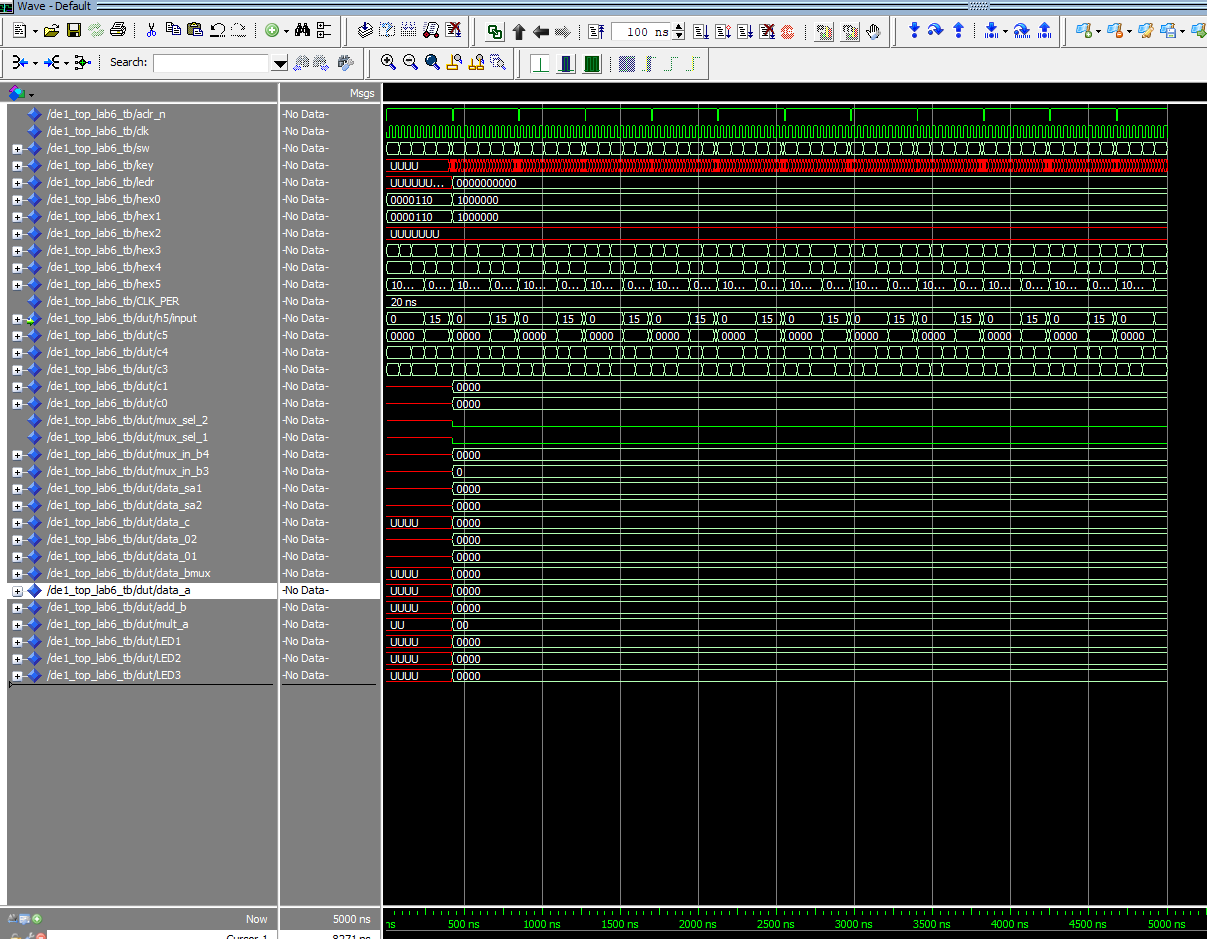
1. For this lab we will be implementing a seven-segment control array controlled by switch inputs, key signals and a LED button.

# Theory of operation:

1. For this design there are multiple requirements.
   1. Signal operations should use TYPE: unsigned
   2. The design takes inputs of type STD\_LOGIC through adders, subtractors and multiplier to display an integer on the seven-segment control’s output.
   3. The input signals are delayed by a shifter controlled by the KEY(0) and KEY(1) signals
   4. Block Diagram:  
      
   5. Some of the limitations of the design
      1. Ways the design can be improved:

# Verification:

1. Test Plan:

We will verify the design by creating a test bench file with predetermined signals. We will create use that file to create a simulation waveform to use in ModelSim.  
  
  
Scenarios objectives included:

* Making sure the asynchronous clear worked
* Making sure the individual components received the proper signals
* Making sure the shifters worked as designed.

# Conclusion:

The most important things taken away from this lab are the flexibility and knowledge for implementing the VHDL language. Also, creating the test vectors that allowed me to simulate real-world actions such as pressing a button or flipping a switch, and what resulted from those actions was a fruitful experience. I struggled with writing the VHDL file within the limitations of the assignment, but it allowed me to better understand exactly what I was doing and more prepared to write safe VHDL. If prompted to start over there are many things that can be implemented a bit neater and the test vectors could have been a bit more comprehensive with a bit of more experience of how the circuit works.